**Lab 1**

**Counter Tutorial**

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**Programmable ASIC Design**

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# Purpose

The purpose of this lab was to introduce students to Xilinx ISE 13.1 and design flow, learn how to specify pin locations, and to become familiar working with the Atlys FPGA board.

# Background

## Atlys FPGA Board

The Atlys board by Digilent, Inc. is a digital circuit development platform based on a Xilinx Spartan-6 LX45 FPGA. The board is fully compatible with all of Xilinx’s CAD software and offers high-end peripherals [1].

Figure . Digilent Atlys FPGA board [1]

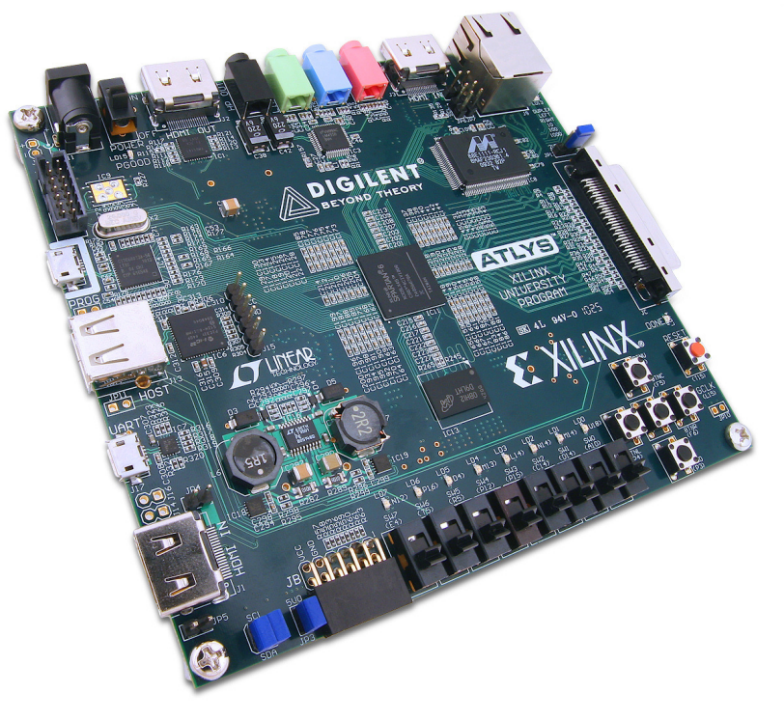
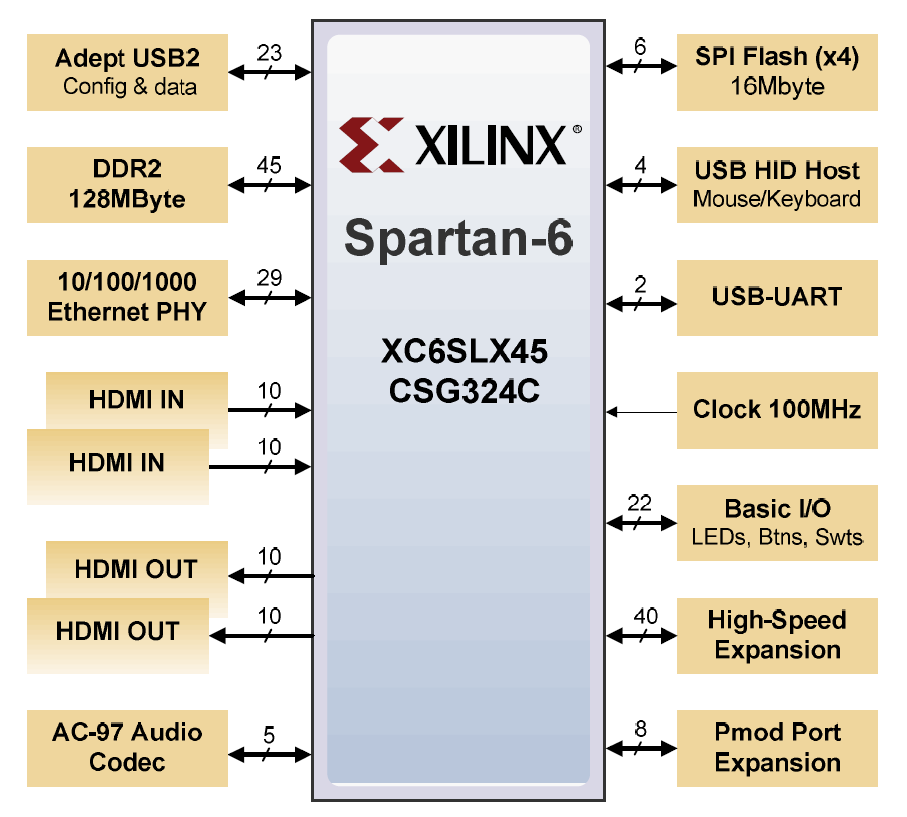


Table . Spartan 6 LX45 specifications [1]

|  |
| --- |
| Specification |
| 6,822 slices, each containing four 6-input LUTs and eight flip-flops |
| 2.1Mbits of fast block RAM |
| Four clock tiles (eight DCMs & four PLLs) |
| Six phase-locked loops |
| 58 DSP slices |
| 500MHz+ clock speeds |

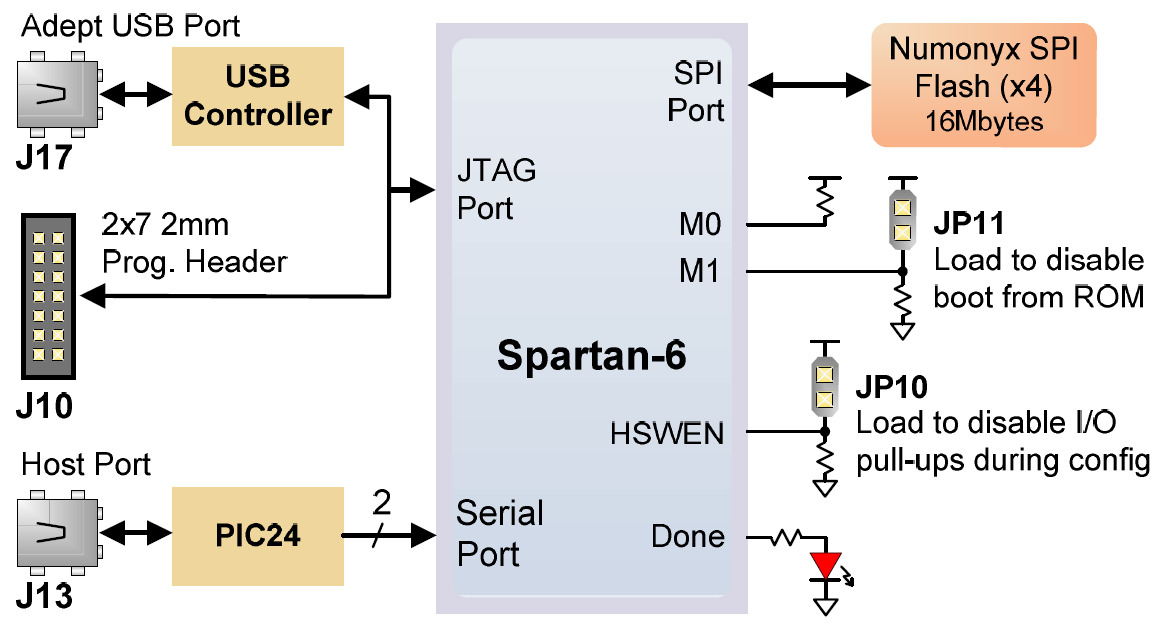
As seen in Figure 2 the Atlys FPGA board offers high-end peripherals, including DDR2 RAM, Ethernet, HDMI IN/OUT, USB, and audio ports. It also has basic I/O, which includes LEDs, buttons, and switches [1].

Figure . Atlys FPGA board architecture [1]



The Atlys board has multiple ways that it can be programmed, from USB/ JTAG, ROM, or USB memory stick. In this lab the USB method is used; however, this can easily be changed by configuring two jumpers that are shown in Figure 3 [1].

Figure . Atlys FPGA board configuration circuit [1]



# Procedure

## Part 1. Counter Tutorial

1. Create a new VHDL project in Xilinx ISE for the Spartan 6 family, XC6SLX45 device, CSG324 package.
2. Create a new VHDL source using the given code.
3. Check for syntax errors.
4. Run Isim to simulate the behavioral model to verify the functionality of the VHDL code.
5. Run PlanAhead to create the user constraint file (.ucf) and set the I/O pins.
6. In PlanAhead set the Site value for the Light[0], Light[1], and Light[2] ports to U18, M14 and N14 respectively. Also, set the Site values for the reset and count up to N4, and P3. (These values were obtained from [1]).
7. Run Synthesize - XST
8. Implement design
   1. Run Translate
   2. Run Map
   3. Run Place & Route
9. Run Generate Programing File, to generate the .bit file.
10. Run the Adept software, which will automatically detect the Atlys board.
11. Select the .bit file that was generated earlier and then click program.

## Part 2. Modify Pin Assignments

1. Modify the ucf file to change the count up and reset inputs to be toggle switches instead of push buttons.
2. Atempted to debounce the count up and reset inputs with adding a clock.

# Results

## Schematics:

Figure . RTL Schematic

Figure . Technology Mapping Schematic

Figure . Place and Route

## Simulations:

Figure . Behavioral Simulation

Figure . Post Synthesis Simulation

Figure . Post Place and Route Simulation

# Discussion of Results

## Part 1

# References

|  |  |
| --- | --- |
| [1] | Digilent, Inc., "Atlys Board Reference Manual," 2 May 2013. [Online]. Available: http://www.digilentinc.com/Data/Products/ATLYS/Atlys\_rm\_V2.pdf. [Accessed 18 February 2015]. |